SONY

CXP83232A/83240A

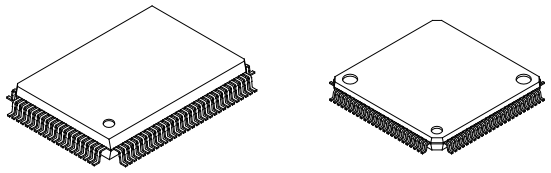
CMOS 8-bit Single Chip Microcomputer

Description

The CXP83232A/83240A is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, 32kHz timer/counter, capture timer counter, LCD controller/driver, remote control reception circuit and 14-bit PWM output besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP83232A/83240A also provides a sleep/stop function that enables lower power consumption.

100 pin QFP (Plastic) 100 pin LQFP (Plastic)



Features

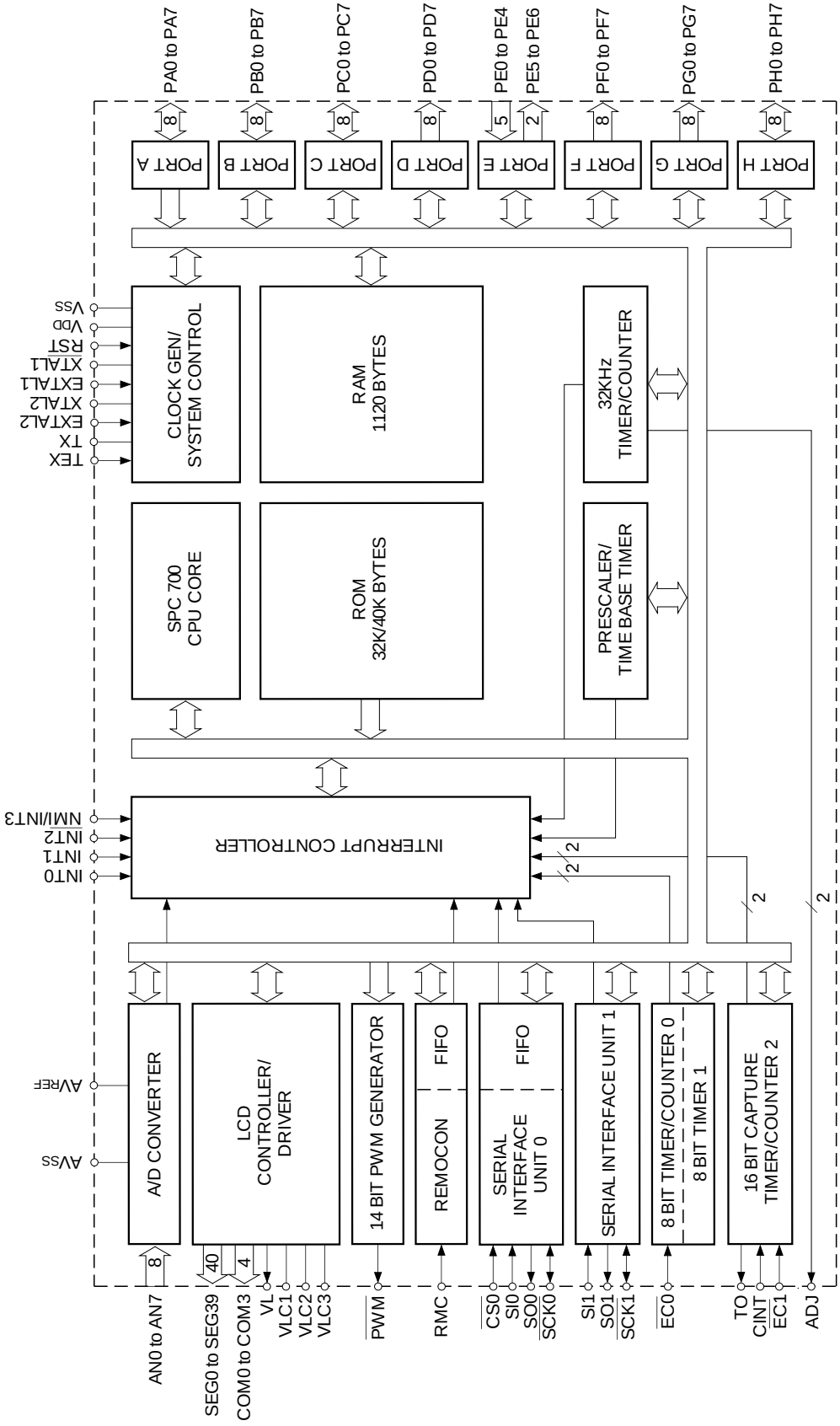
- Wide-range instruction system (213 instructions) to cover various types of data.
  - — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle 400ns at 10MHz operation
  8µs at 500kHz
  122µs at 32kHz operation
- Incorporated ROM capacity 32Kbytes (CXP83232A)
  40Kbytes (CXP83240A)
- Incorporated RAM capacity 1120bytes (includes LCD display data area)
- Peripheral functions
  - — A/D converter 8-bit, 8-channel, successive approximation method
    (Conversion time of 32µs/10MHz)
  - — Serial interface 8-bit, 8-stage FIFO incorporated
    (Auto transfer for 1 to 8 bytes), 1 channel
    8-bit clock synchronized type, 1 channel
  - — Timer 8-bit timer, 8-bit timer/counter, 19-bit time base timer,
    16-bit capture timer/counter, 32kHz timer/counter
  - — LCD controller/driver Maximum 160 segment display possible (during 1/4 duty)
    4 common output, 40 segment output
    Display method static, 1/2, 1/3, 1/4 duty
    Bias method 1/2, 1/3 bias
  - — Remote control reception circuit 8-bit pulse measuring counter, 6-stage FIFO
  - — PWM output circuit 14 bits, 1 channel
- Interruption 15 factors, 15 vectors, multi-interruption possible
- Standby mode SLEEP/STOP
- Package 100-pin plastic QFP/LQFP
- Piggyback/evaluation chip CXP83200A 100-pin ceramic QFP/LQFP

Structure

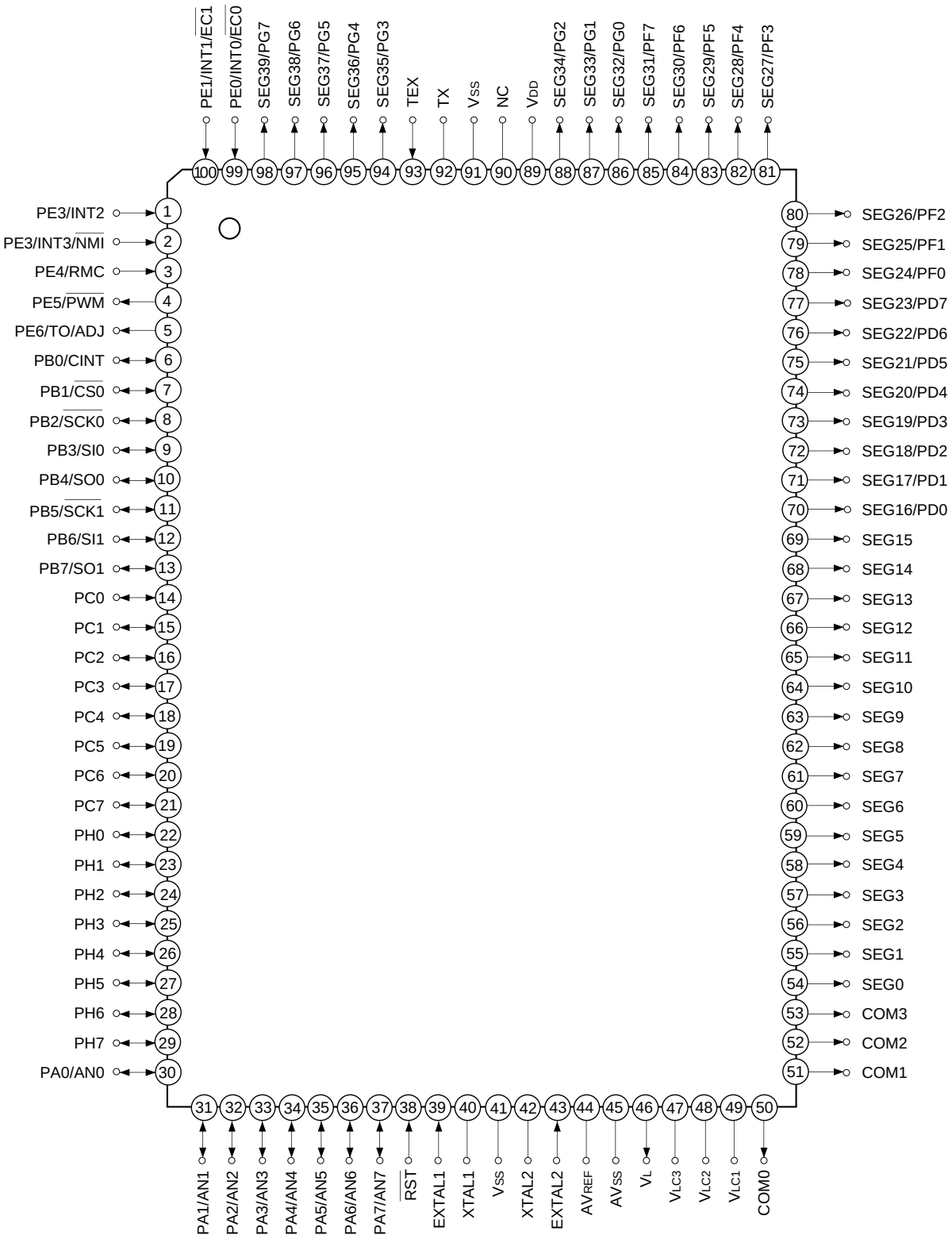
Silicon gate CMOS IC

E94842-PP

Block Diagram

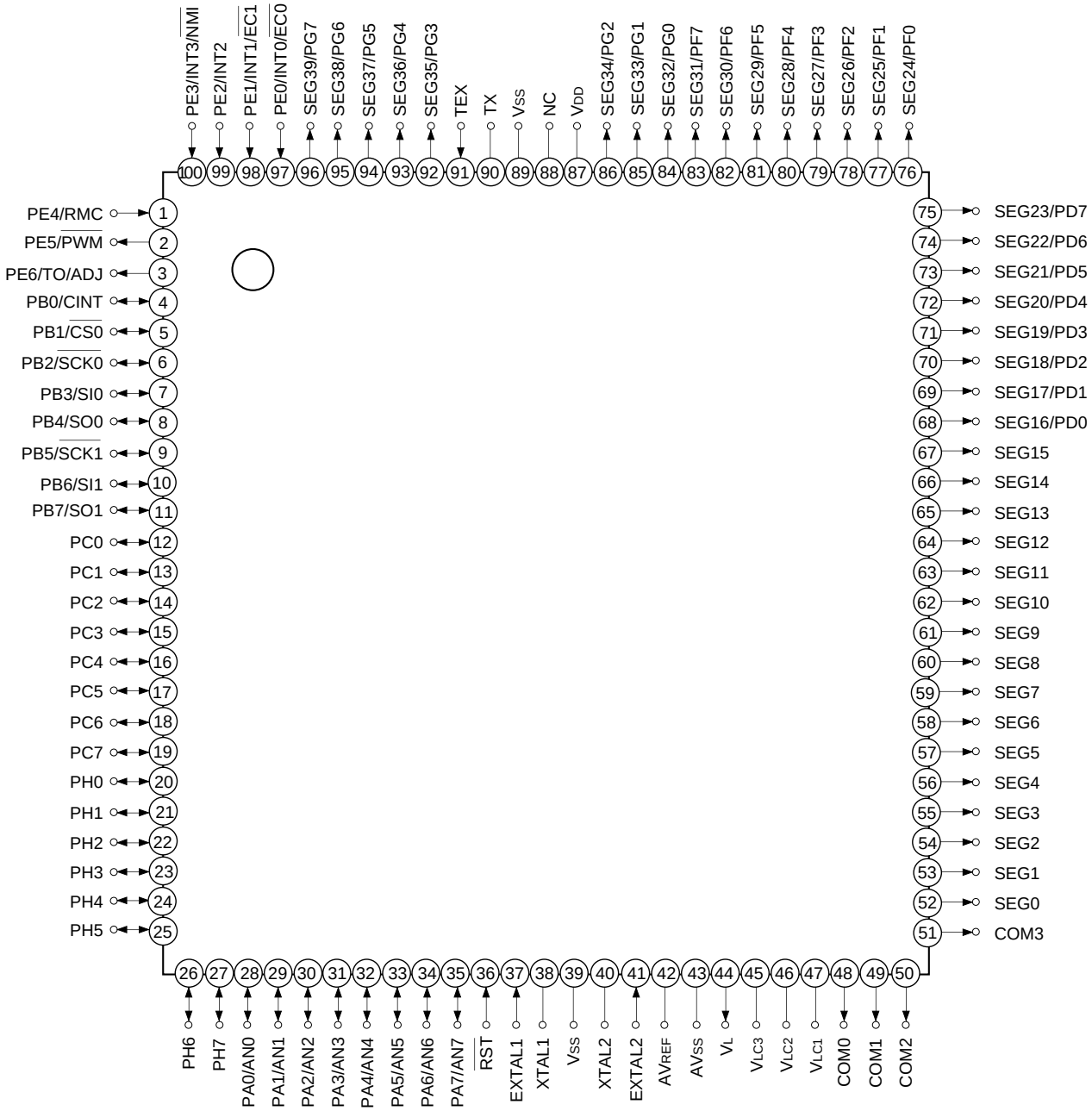


Pin Assignment (Top View) (QFP package)



Note) 1. NC (Pin 90) is always connected to V_{DD}.
2. V_{SS} (Pin 41 and 91) are both connected to GND.

Pin Assignment (Top View) (LQFP package)



Note) 1. NC (Pin 88) is always connected to V_{DD}.

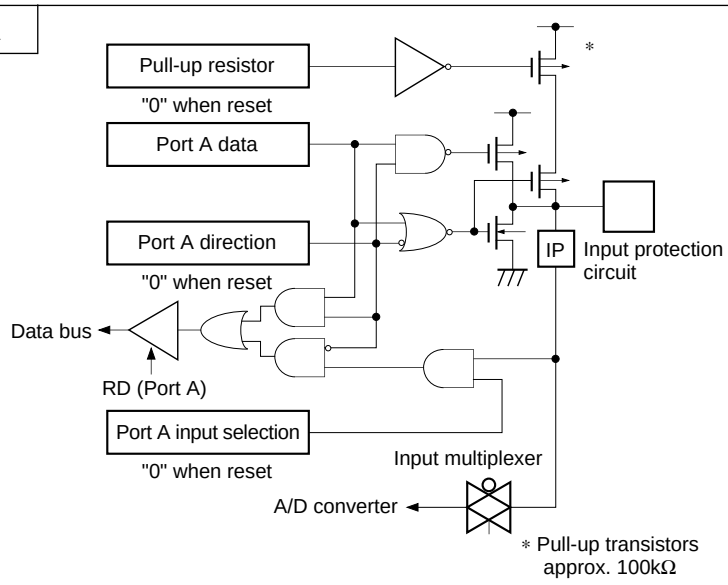
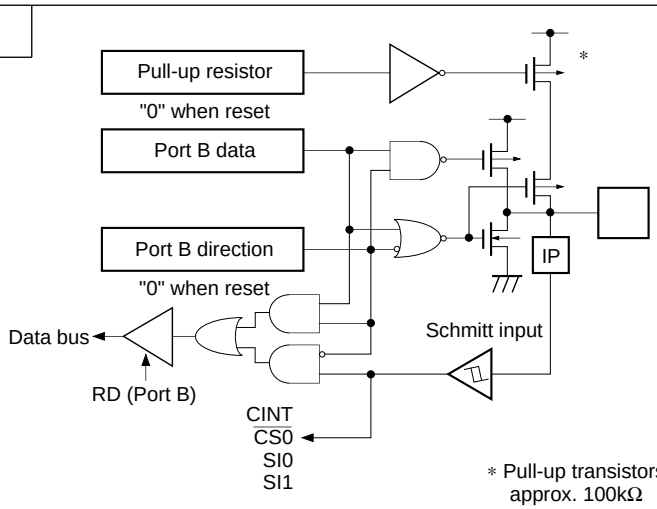
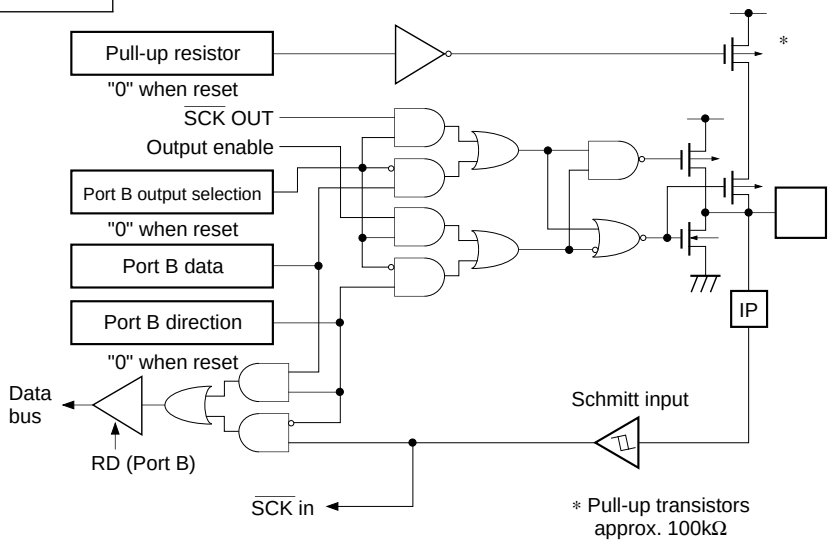
2. V_{SS} (Pin 39 and 89) are both connected to GND.

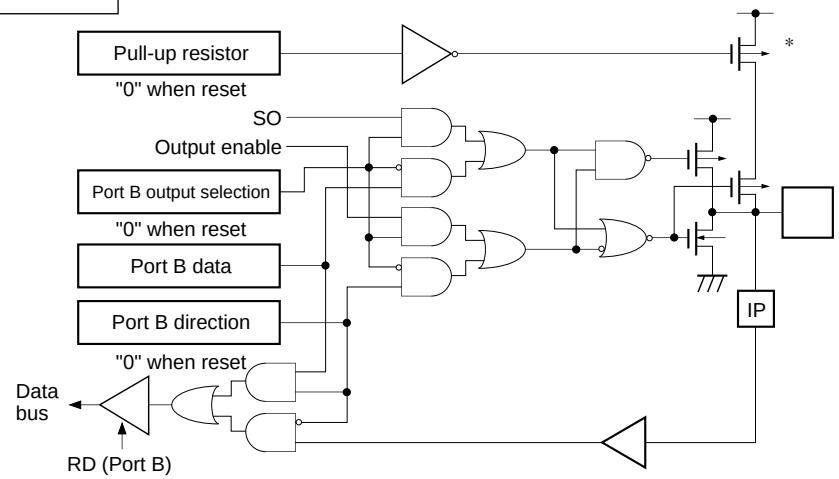
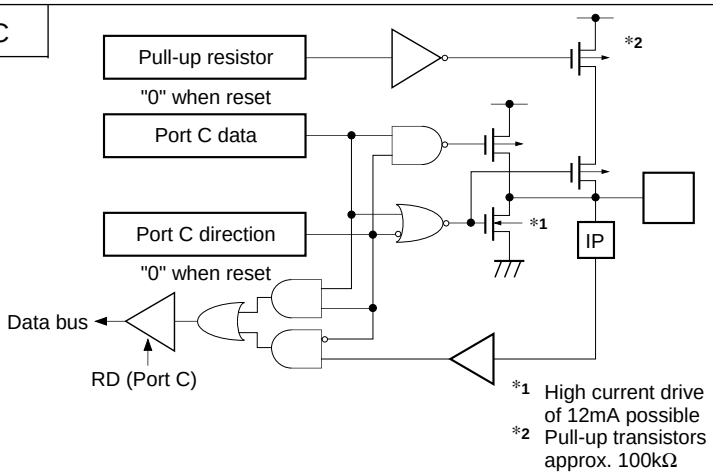
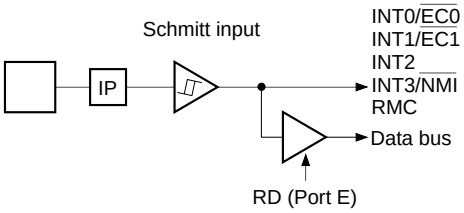
Pin Description

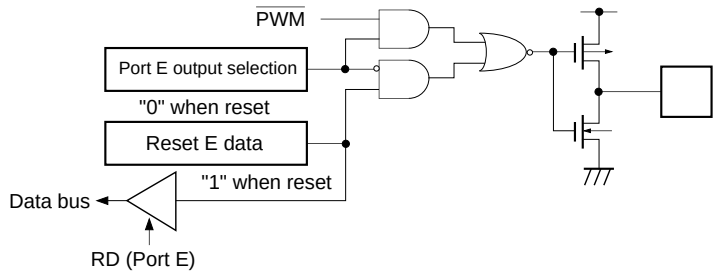
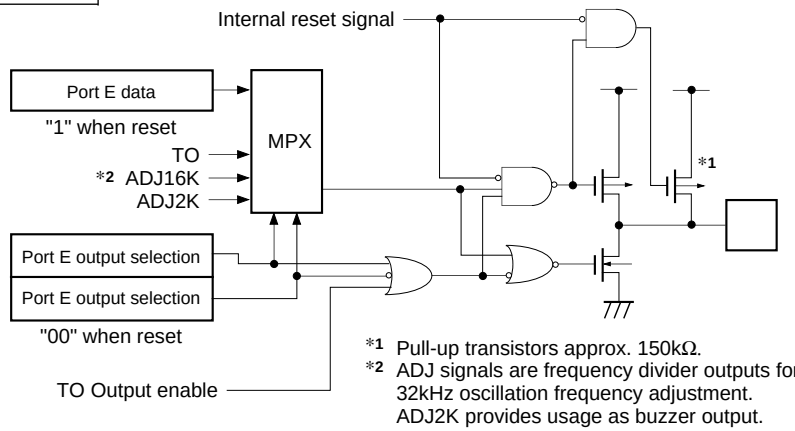
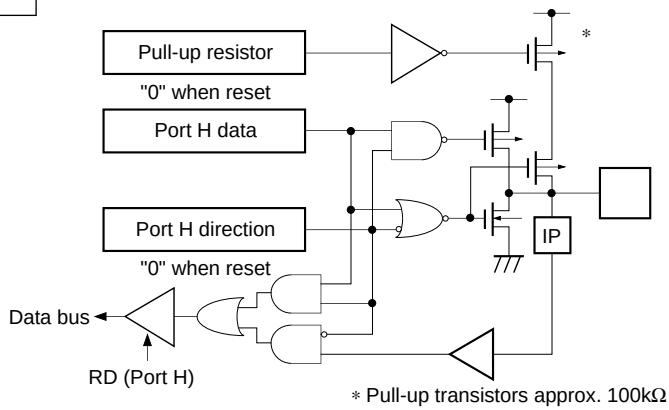
Symbol	I/O	Functions		
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a single bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)	
PB0/CINT	I/O/Input	(Port B) 8-bit I/O port. I/O can be set in a single bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External capture input to 16-bit timer/counter.	
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).	
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).	
PB3/SI0	I/O/Input		Serial data input (CH0).	
PB4/SO0	I/O/Output		Serial data output (CH0).	
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).	
PB6/SI1	I/O/input		Serial data input (CH1).	
PB7/SO1	I/O/Output		Serial data output (CH1).	
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a single bit unit. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)		
$\overline{PE0}$/INT0/ $\overline{EC0}$	Input/Input/Input	(Port E) 7-bit port. lower 5 bits are for inputs; upper 2 bits are for outputs. (7 pins)	External event inputs for timer/counter. (2 pins)	
$\overline{PE1}$/INT1/ $\overline{EC1}$	Input/Input/Input			
PE2/INT2	Input/Input		External interruption request inputs. (4 pins)	
$\overline{PE3}$/INT3/ $\overline{NMI}$	Input/Input/Input			Non-maskable interruption request input.
PE4/RMC	Input/Input		Remote control reception circuit input.	
PE5/$\overline{PWM}$	Output/Output		14-bit PWM output.	
PE6/TO/ ADJ	Output/Output/ Output		Rectangular wave output for 16-bit timer/counter (duty output 50%).	Output for 32kHz oscillation frequency division.
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a single bit unit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)		

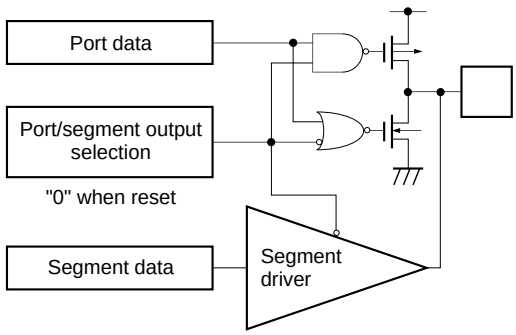
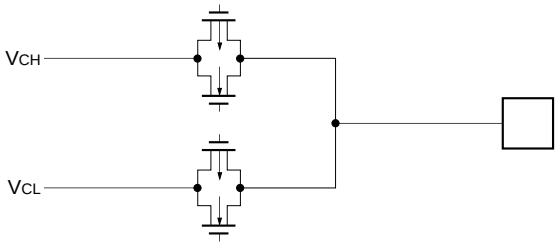
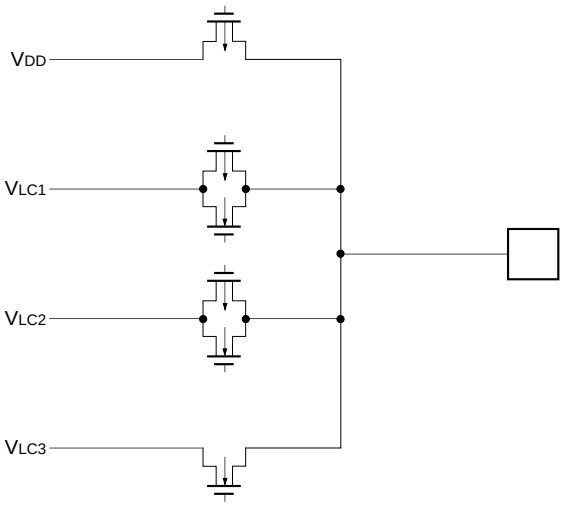
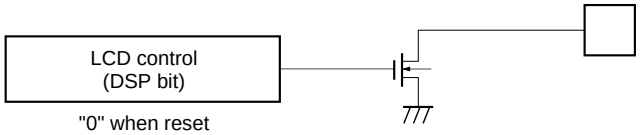
Symbol	I/O	Functions	
PD0/SEG16 to PD7/SEG23	Output/Output	(Port D) 8-bit output port. (8 pins)	LCD segment signal output.
PF0/SEG24 to PF7/SEG31	Output/Output	(Port F) 8-bit output port. (8 pins)	
PG0/SEG32 to PG7/SEG39	Output/Output	(port G) 8-bit output port. (8 pins)	
SEG0 to SEG15	Output	LCD segment signal output.	
COM0 to COM3	Output	LCD common signal output.	
V_{LC1} to V_{LC3}		LCD bias power supply.	
V_L	Output	Control pin to cut off the current flowing to external LCD bias resistor during standby.	
EXTAL1	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL1; opposite phase clock should be input to XTAL1. System clock oscillation of EXTAL1 and XTAL1 is used for normal operation mode (Max. 10MHz).	
XTAL1			
EXTAL2	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL2; opposite phase clock should be input to XTAL2. System clock oscillation of EXTAL2 and XTAL2 is used for sub clock mode (Typ. 500kHz).	
XTAL2			
TEX	Input	Crystal connectors for 32kHz timer/counter clock generation circuit. Connect a 32.768kHz crystal oscillator between TEX and TX. For usage as event input, connect clock oscillation source to TEX, and leave TX open.	
TX	Output		
$\overline{RST}$	Input	Low-level active system reset.	
NC		NC. Under normal operating conditions, connect to V_{DD}.	
AV_{REF}	Input	Reference voltage input for A/D converter.	
AV_{SS}		A/D converter GND.	
V_{DD}		Positive power supply.	
V_{SS}		GND. Two V_{SS} are connected to GND.	

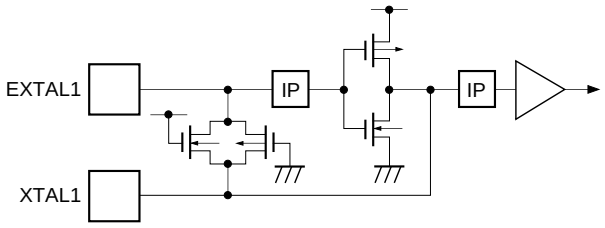
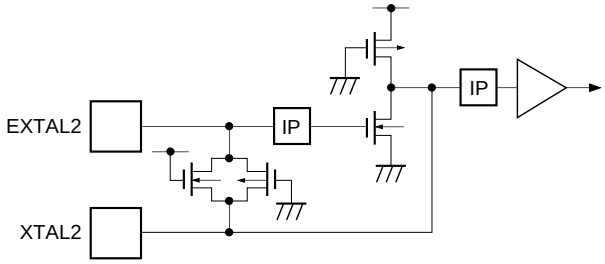
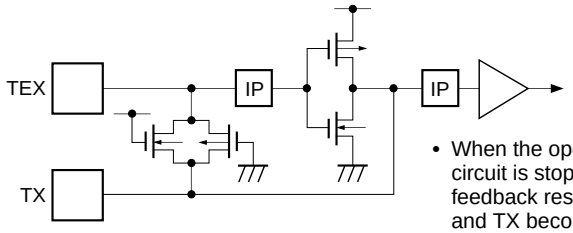
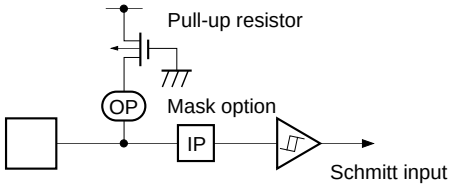
I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	Port A 	Hi-Z
PB0/$\overline{\text{CINT}}$ PB1/$\overline{\text{CS0}}$ PB3/SI0 PB6/SI1 4 pins	Port B 	Hi-Z
PB2/$\overline{\text{SCK0}}$ PB5/SCK1	Port B 	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 PB7/SO1 2 pins	Port B 	Hi-Z
PC0 to PC7 8 pins	Port C 	Hi-Z
PE0/INT0/$\overline{EC0}$ PE1/INT1/EC1 PE2/INT2 $\overline{\quad}$ PE3/INT3/$\overline{NMI}$ PE4/RMC 5 pins	Port E 	Hi-Z

Pin	Circuit format	When reset
PE5/$\overline{PWM}$ 1 pin	Port E 	High level
PE6/TO/ADJ 1 pin	Port E  *1 Pull-up transistors approx. 150kΩ. *2 ADJ signals are frequency divider outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.	High level (High level with 150kΩ resistor when reset)
PH0 to PH7 8 pins	Port H  * Pull-up transistors approx. 100kΩ	Hi-Z

Pin	Circuit format	When reset
PD0 to PD7 PF0 to PF7 PG0 to PG7 24pins	Port D Port F Port G PD7 to PD4 by a single bit unit PD3 to PD0 by 4-bit unit PF7 to PF0 PG7 to PG0 by 8-bit unit 	Segment output (V_{DD} level)
SEG0 to SEG15 16 pins	Segment 	V_{DD} level
COM0 to COM3 4 pins	Common 	V_{DD} level
V_L 1 pin		Hi-Z

Pin	Circuit format	When reset
EXTAL1 XTAL1 2 pins	 • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop. XTAL1 becomes "High" level.	Oscillation
EXTAL2 XTAL2 2 pins	 • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop. XTAL2 becomes "High" level.	EXTAL2 Hi-Z XTAL2 High level
TEX TX 2 pins	 • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed and TEX and TX become "Low" level and "High" level respectively.	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	AV_{SS}	–0.3 to +0.3	V	
LCD bias voltage	V_{LC1}, V_{LC2}, V_{LC3}	–0.3 to +7.0*1	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
High level output current	I_{OH}	–5	mA	Output per pin
High level total output current	$\sum I_{OH}$	–50	mA	Total for all output pins
Low level output current	I_{OL}	15	mA	Value per pin, excluding high current outputs
	I_{OLC}	20	mA	Value per pin*2 for high current outputs
Low level total output current	$\sum I_{OL}$	100	mA	Total for all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP package
		380		LQFP package

*1 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 The high current drive transistor is the N-ch transistor of Port C (PC)

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	High-speed mode guaranteed operation range*1
		3.5	5.5		Low-speed mode guaranteed operation range*1
		3.0	5.5		Guaranteed operation range during EXTAL2 clock (sub clock mode)
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during STOP
LCD bias voltage	V_{LC1}	Vss	V_{DD}	V	LCD power supply range*5
	V_{LC2}				
	V_{LC3}				
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	*2
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	Hysteresis input*3
	V_{IHEX}	$V_{DD} - 0.4$	$V_{DD} + 0.3$	V	EXTAL*4
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	*2
	V_{ILS}	0	$0.2V_{DD}$	V	Hysteresis input*3
	V_{ILEX}	–0.3	0.4	V	EXTAL*4
Operating temperature	Topr	–20	+75	°C	

*1 During EXTAL1 clock (main clock mode), high-speed mode is 1/2 frequency division clock selection; low-speed mode is 1/16 frequency division clock selection.

*2 Value for each pin of normal input ports (PA, PB4, PB7, PC and PH).

*3 Value of the following pins; $\overline{RST}$, CINT $\overline{CS0}$, SI0, SI1, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{EC0}$/INT0, $\overline{EC1}$/INT1, INT2, $\overline{NMI}$/INT3, and RMC.

*4 Specifies only during external clock input.

*5 Optimal values are determined by LCD used.

Electrical Characteristics

DC Characteristics

(Ta = –20 to +75°C, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA, PB, PC, PD*1, PE5, PE6 PF to PG*1 V_L (only V_{OL})	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE1}	EXTAL1	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE1}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHE2}	EXTAL2	V_{DD} = 5.5V, V_{IH} = 5.5V	0.3		30	µA
	I_{ILE2}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.3		–30	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*2	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
	I_{IH}	PA to PC*3, PH*3 PE0 to PE4, $\overline{RST}$*2	V_{DD} = 4.5V, V_{IH} = 4.0V	–3.33			µA
	I_{IL}		V_{DD} = 5.5V, V_{IL} = 0.4V			–50	µA
I/O leakage current	I_{IZ}		V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Common output impedance	R_{COM}	COM0 to COM3	V_{DD} = 5V, V_{LC1} = 3.75V V_{LC2} = 2.5V V_{LC3} = 1.25		3	5	kΩ
Segment output impedance	R_{SEG}	SEG0 to SEG15 SEG16 to SEG39*1			5	15	kΩ
Supply current*4	I_{DD1}	V_{DD}	High-speed mode operation (1/2 frequency division clock) V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		20	45	mA
	I_{DD2}		V_{DD} = 3.5V, 500kHz crystal oscillation (C_1 = C_2 = 22pF)		0.9	2.2	mA
	I_{DD3}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		35	100	µA
	I_{DDS1}		SLEEP mode V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		1.5	8	mA
	I_{DDS2}		V_{DD} = 3.5V, 500kHz crystal oscillation (C_1 = C_2 = 22pF)		450	900	µA
	I_{DDS3}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		9	30	µA
	I_{DDSS}		STOP mode V_{DD} = 5.5V, 10MHz, 500kHz crystal oscillation and termination of 32kHz oscillation			10	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacity	C_{IN}	Pins other than PB7, PE5, PE6 V_{LC1} to V_{LC3} COM0 to COM3 SEG0 to SEG15 PD0/SEG16 to PD7/SEG23 PF0/SEG24 to PF7/SEG31 PG0/SEG32 to PG7/SEG39 AV_{REF}, AV_{SS}, V_{DD}, V_{SS}	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 Common pins of PD0/SEG16 to PD7/SEG23, PF0/SEG24 to PF7/SEG31, PG0/SEG32 to PG7/SEG39, PD, PF and PG is the case when the common pin is selected as port; SEG16 to SEG39 is when the common pin is selected as segment output.

*2 $\overline{RST}$ specifies the input current when pull-up resitor has been selected; leakage current when no resistor has been selected.

*3 Pins PA to PC, and PH specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected. (PE0 to PE4 specifies the leakage current.)

*4 When all output pins are left open.

AC Characteristics

(1) Clock timing

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL1 EXTAL1	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL1	Fig. 1, Fig. 2 external clock drive	37.5			ns
System clock input rise and fall time	t_{CR}, t_{CF}	EXTAL1	Fig. 1, Fig. 2 external clock drive			200	ns
System clock frequency	f_C	XTAL2 EXTAL2	V_{DD} = 3.0 to 5.5V Fig. 1, Fig. 2	0.3	0.5	0.7	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL2	V_{DD} = 3.0 to 5.5V Fig. 1, Fig. 2 external clock drive	450			ns
System clock input rise and fall time	t_{CR}, t_{CF}	EXTAL2	V_{DD} = 3.0 to 5.5V Fig. 1, Fig. 2 external clock drive			200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC0}$ EC1	Fig. 3	$t_{sys}+50$*			ns
Event count input clock rise and fall time	t_{ER}, t_{EF}	$\overline{EC0}$ EC1	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count input clock rise and fall time	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

* t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FE$_H$).
t_{sys} (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11").

Fig. 1. Clock timing

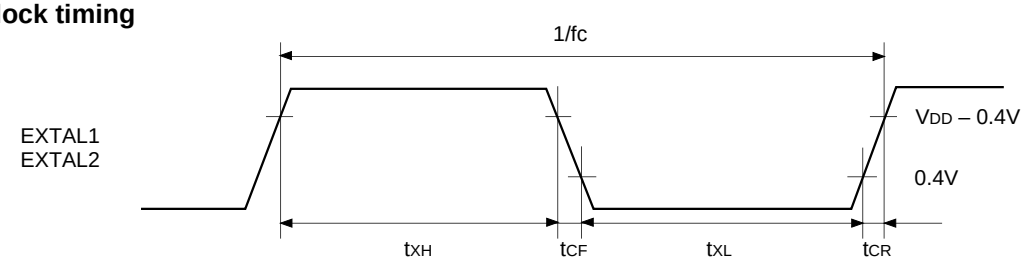


Fig. 2. Clock applied conditions

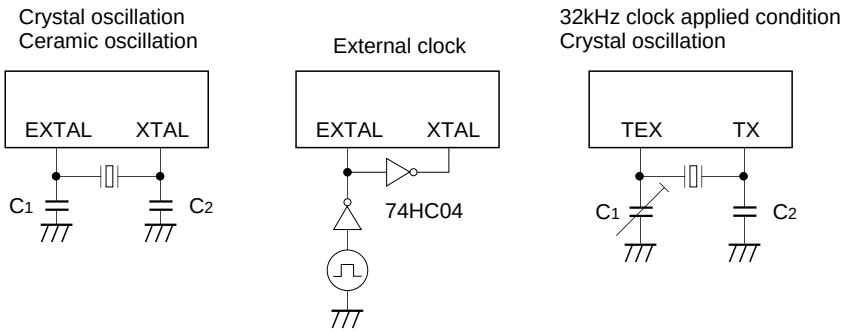
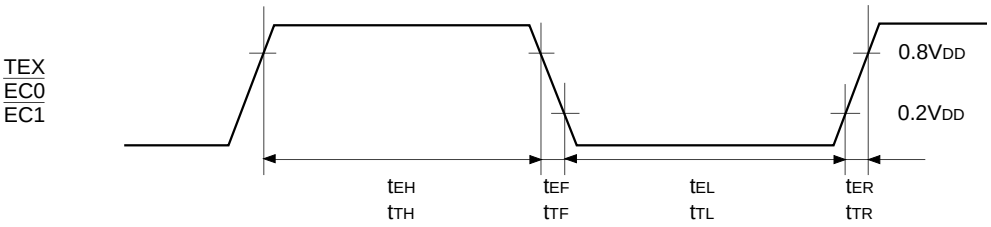


Fig. 3. Event count clock timing



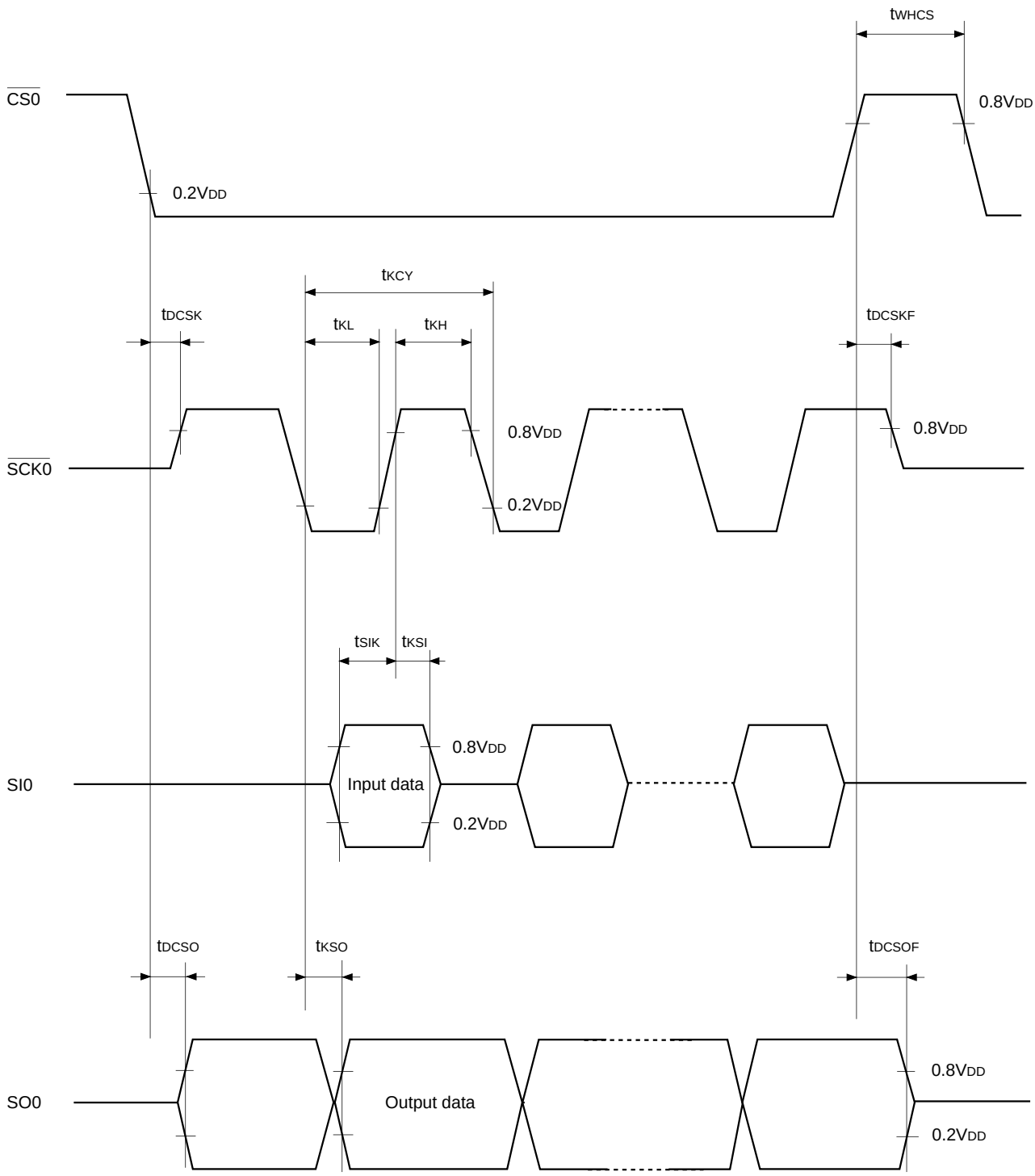
(2) Serial transfer (CH0) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \downarrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow$ SO0 float delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 50		ns
SI0 input setup time (for $\overline{SCK0} \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys + 200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FE$_H$).
tsys (ns) = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01", 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing

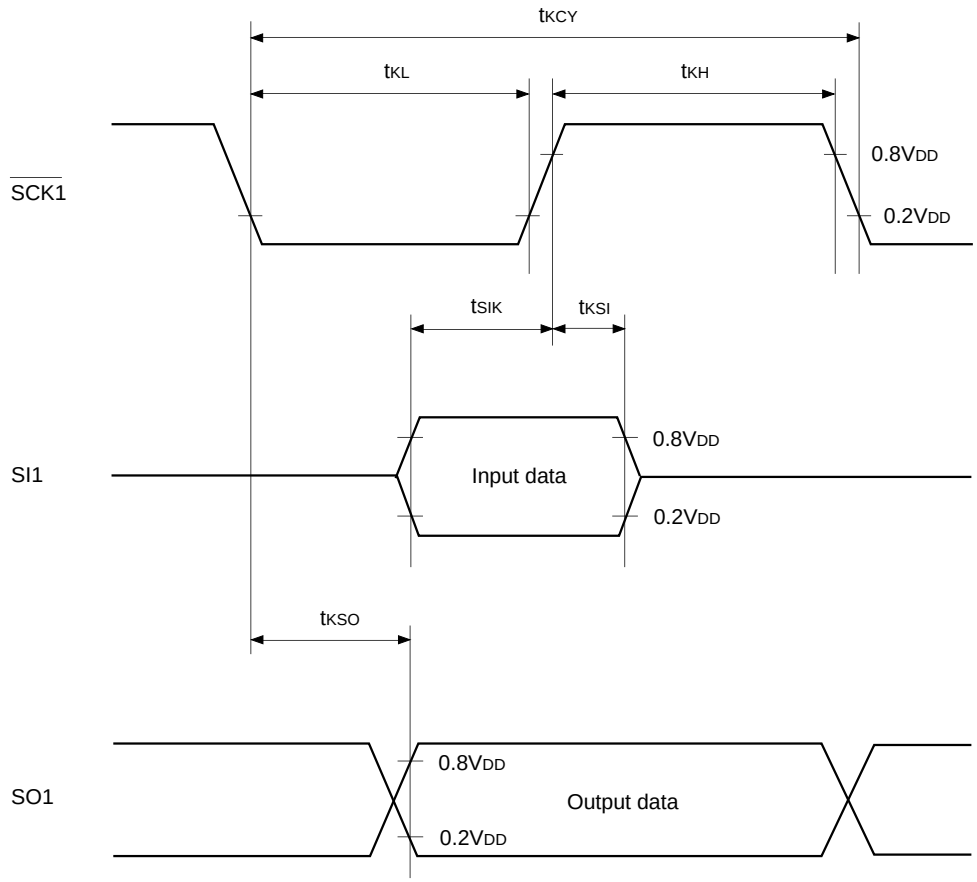


Serial Transfer (CH1) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	input mode	400		ns
			Output mode	8000/fc – 50		ns
SI1 input setup time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		200	ns
			$\overline{SCK1}$ output mode		100	ns

Note) The load condition for the $\overline{SCK1}$ output mode, SO1 output delay time is 50pF + 1TTL.

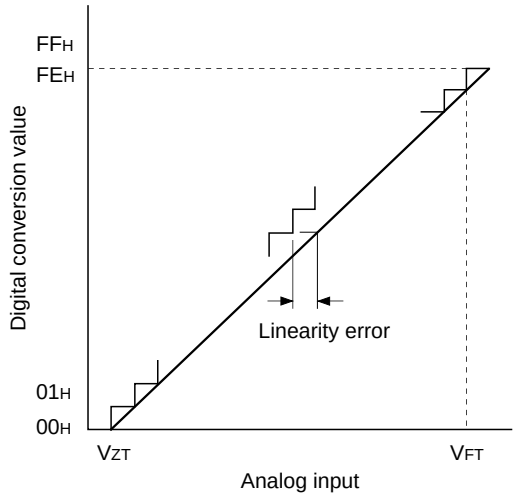
Fig. 5. Serial transfer CH1 timing



(3) A/D converter characteristics (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = AV_{SS} = 0V)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–10	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			µs
Sampling time	t_{SAMP}			12/f_{ADC}*3			µs
Reference input voltage	V_{REF}	AV_{REF}		V_{DD} – 0.5		V_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operation mode			10	µA

Fig. 6. Definition of A/D converter terms



*1 V_{ZT}: Value at which the digital conversion value changes from 00_H to 01_H and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FE_H to FF_H and vice versa.

*3 f_{ADC} indicates the below values due to the Bit 6 (CKS) of A/D control register (address: $00F9_H$) and the Bit 7 (PCK1) and Bit 6 (PCK0) of clock control register (address: $00FF_H$).

CKS / PCK1, PCK0	0 (ϕ/2 selection)	1 (ϕ selection)
00 (ϕ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (ϕ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (ϕ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	INT0 INT1 INT2 NMI/INT3		1		µs
Reset input low level width	t_{RSL}	RST		32/fc		µs

Fig. 7. Interruption input timing

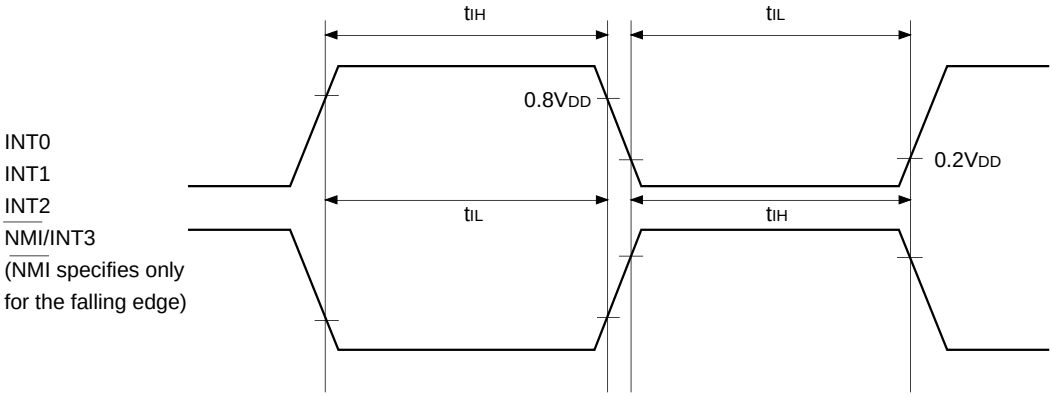
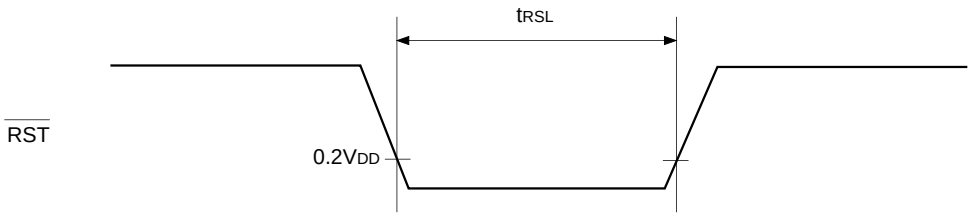
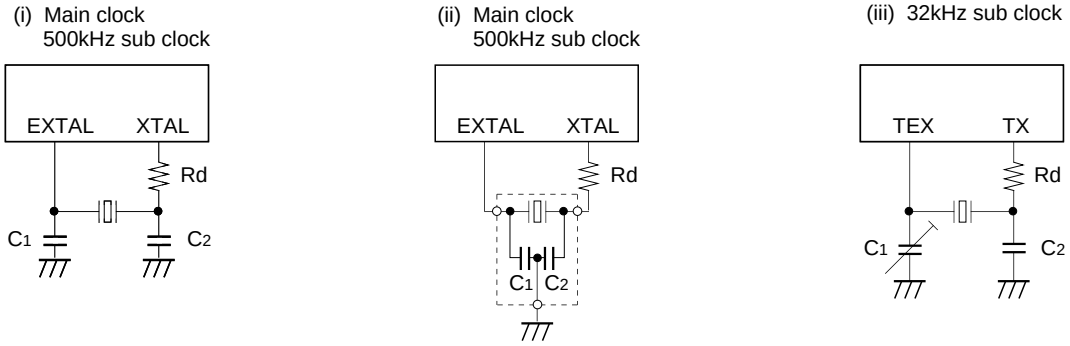


Fig. 8. RST input timing



Appendix

Fig. 9. SPC700 series recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MG	8.00				
	CSA10.0MT	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.00MTW*	10.00				
RIVER ELETEC CO., LTD.	HC-49/U03	4.19	15	15	2.2k	(i)
		8.00				
		10.00			470	
KINSEKI LTD.	HC-49/U (-S)	4.19	22	22	560	
		8.00	18	18	0	
		10.00				

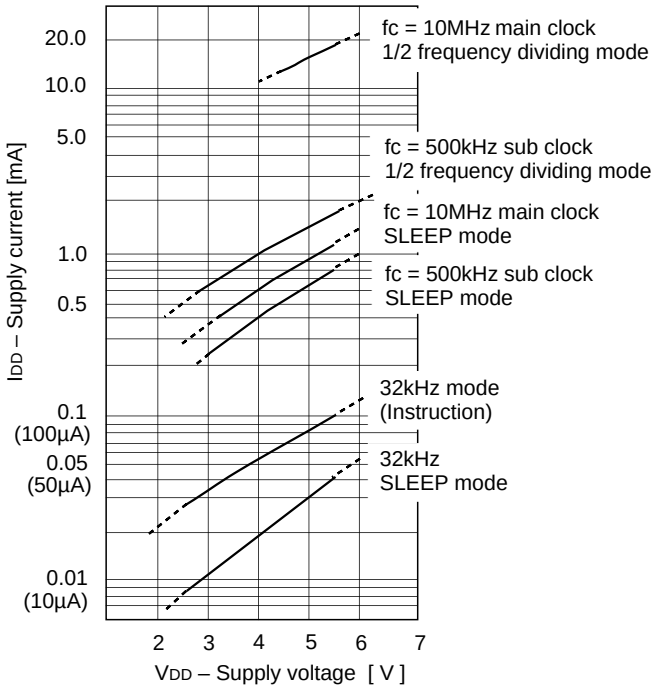
Those marked with an asterisk (*) signify types with built-in ground capacitance (C_1, C_2).

Mask Option Table

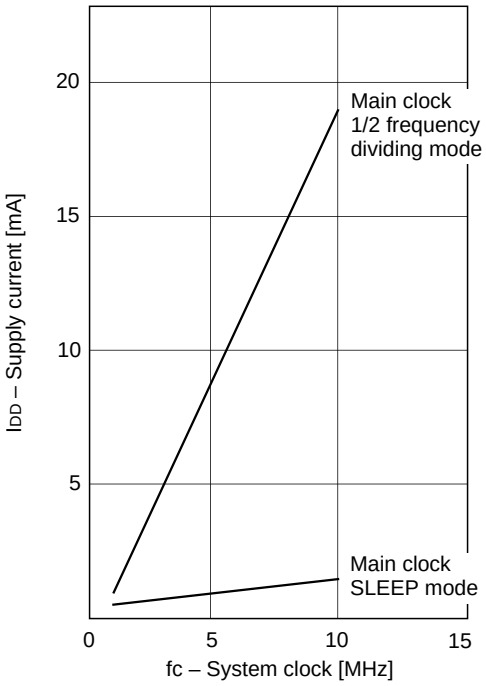
Item	Content	
Reset pin pull-up resistor	Non-existent	Existent

Characteristics Curves

IDD vs. VDD
(Ta = 25°C, typical)



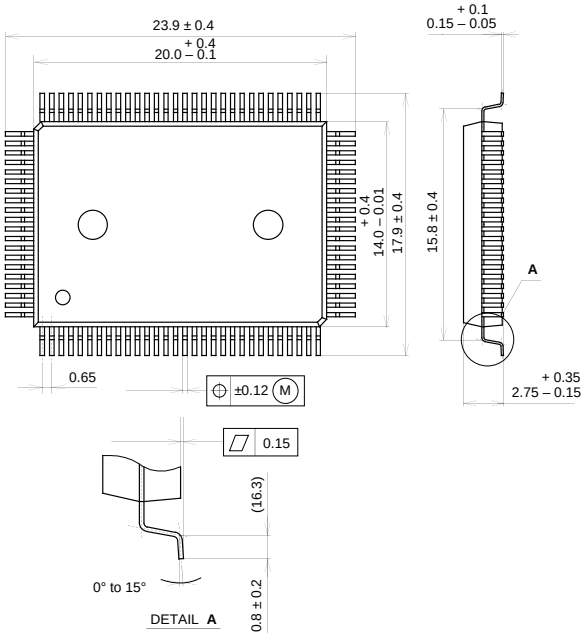
IDD vs. fc
(VDD = 5V, Ta = 25°C, typical)



Package Outline

Unit: mm

100PIN QFP (PLASTIC)

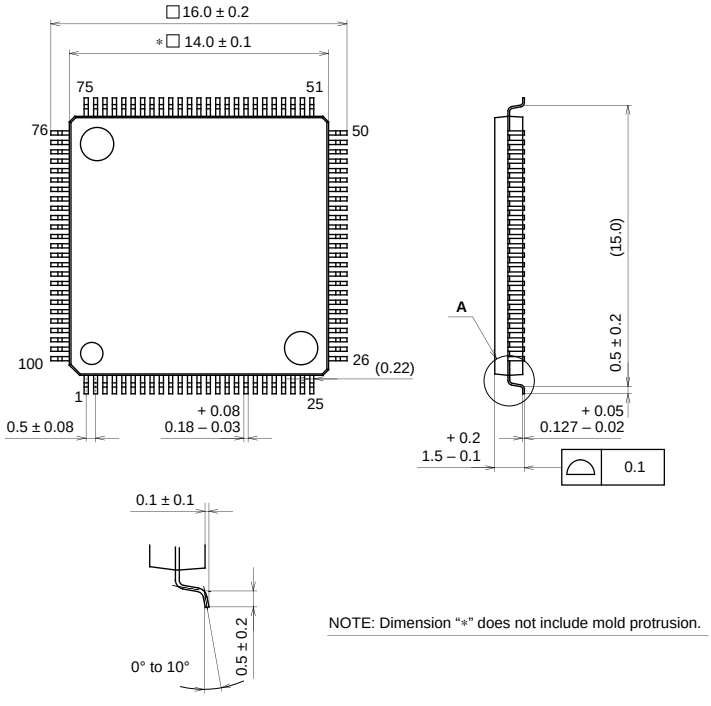


SONY CODE	QFP-100P-L01
EIAJ CODE	∗QFP100-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g

100PIN LQFP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	∗QFP100-P-1414-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY/PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	————